

INTRODUCTION

This project looks to provide Radio Frequency (RF) spectral situational awareness, focusing on the Internet of Things (IoT) protocol LoRa.

AIM

The aims of this work are to develop a RF situational awareness capability based around the RF System on a Chip (RFSoc) (Fig 1b). The solution looks to operate with automatic detect and classify capabilities. The ability to extract both when a signal has been detected as well as its exact waveform parameters is described. An example LoRa device is shown in Fig 1a.

DEVELOPMENTS

- UCL's highly flexible ARESTOR RF sensor platform has been enhanced to provide real-time monitoring and characterization of LoRa signals.
- FPGA hardware based channelisation of the 8 MHz LoRa frequency span, dividing the bandwidth into multiple overlapping regions of 500 kHz each.
- Hardware FFT implementation to create time-frequency representations of signals in each channel.
- SIMD software implementation of Hough transform and LoRa parameter extraction.

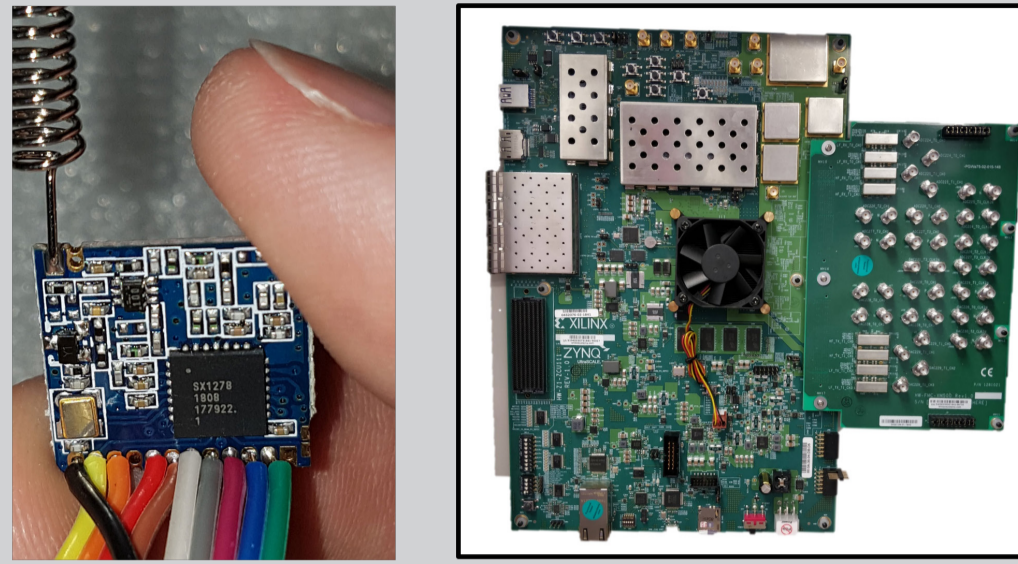


Fig 1: a) LoRa device b) RFSoc Development Board

METHODOLOGY

This project uses a RFSoc device (Fig 1b) to capture RF signals. This high sample rate device is able to directly sample the signals of interest. The LoRa protocol is at ~868 MHz and has a series of different parameters for each signal. These include central frequency, spreading factor and bandwidth. The structure of the LoRa transmission in the time-frequency domain is shown in Fig 2.

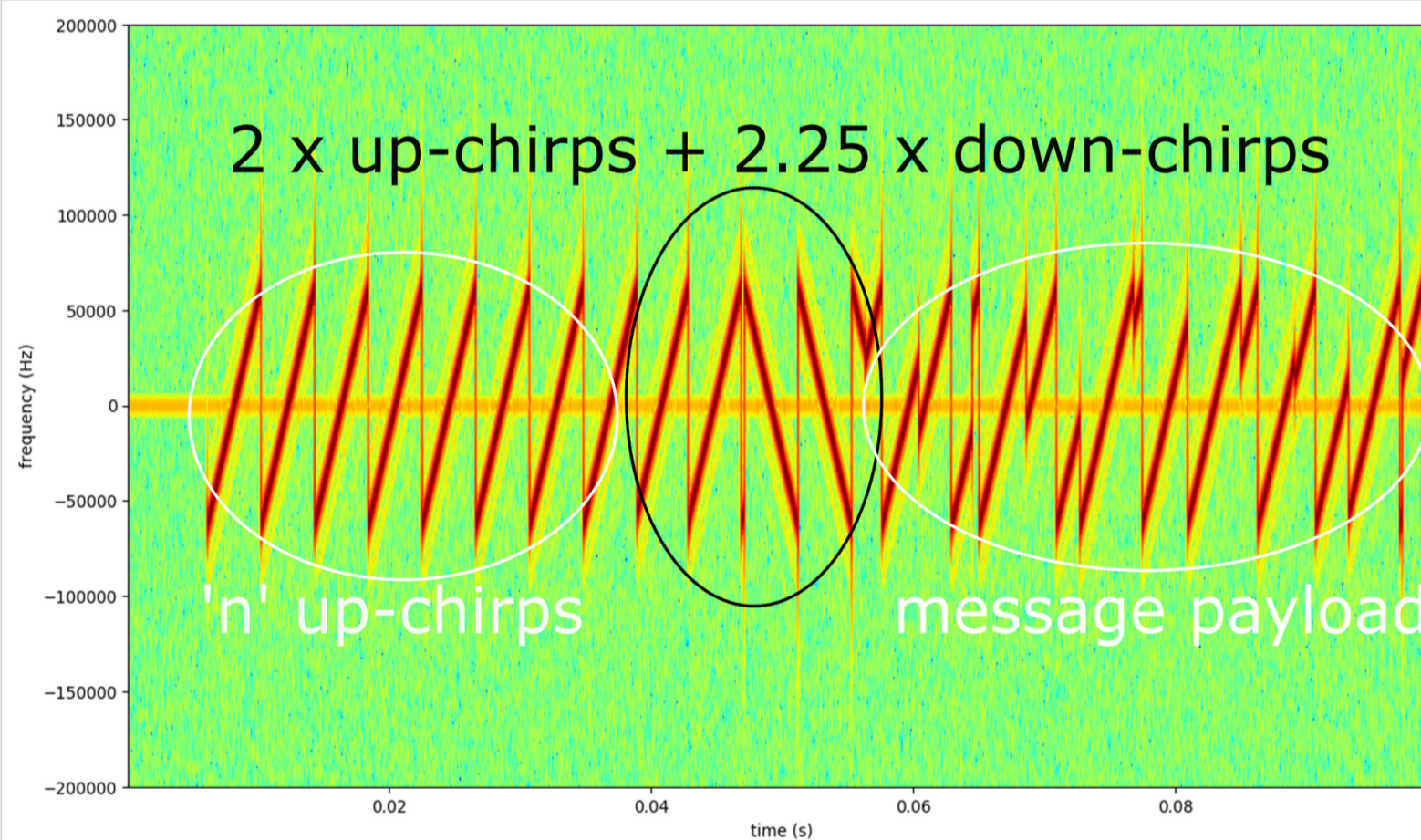


Fig 2: Example LoRa signal

The approach taken to detect and characterise LoRa signals is based on image processing techniques applied to the time-frequency representation (TF). The two full downchirps seen in Fig 2 are isolated using the Hough transform applied to a thinned, binary version of the original TF. An example TF binary image prior to thinning is shown in Fig 3.

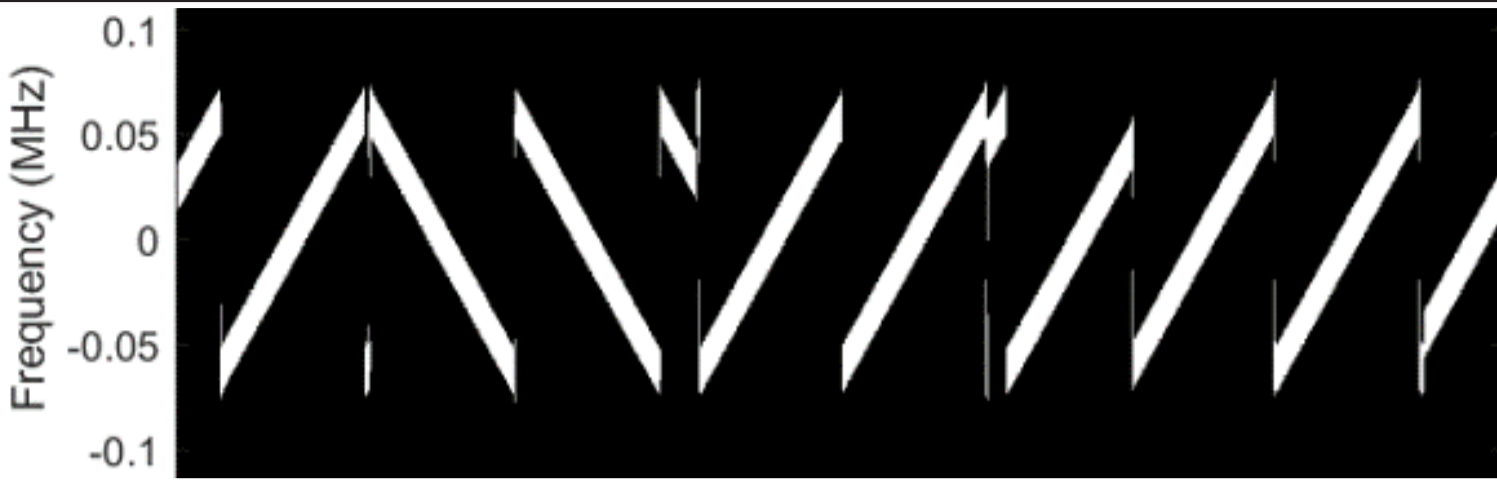


Fig 3: Binary Time-Frequency Representation of LoRa

The identified downchirps (green lines in Fig 4) are matched against the original thinned image to identify the frequency extent. The gradient of the downchirps along with their frequency extent enables estimation of bandwidth and spreading factor of the detected LoRa transmission. The centre frequency f_c of the signal is determined from the mid point of the chirp and the channel in which the signal is detected.

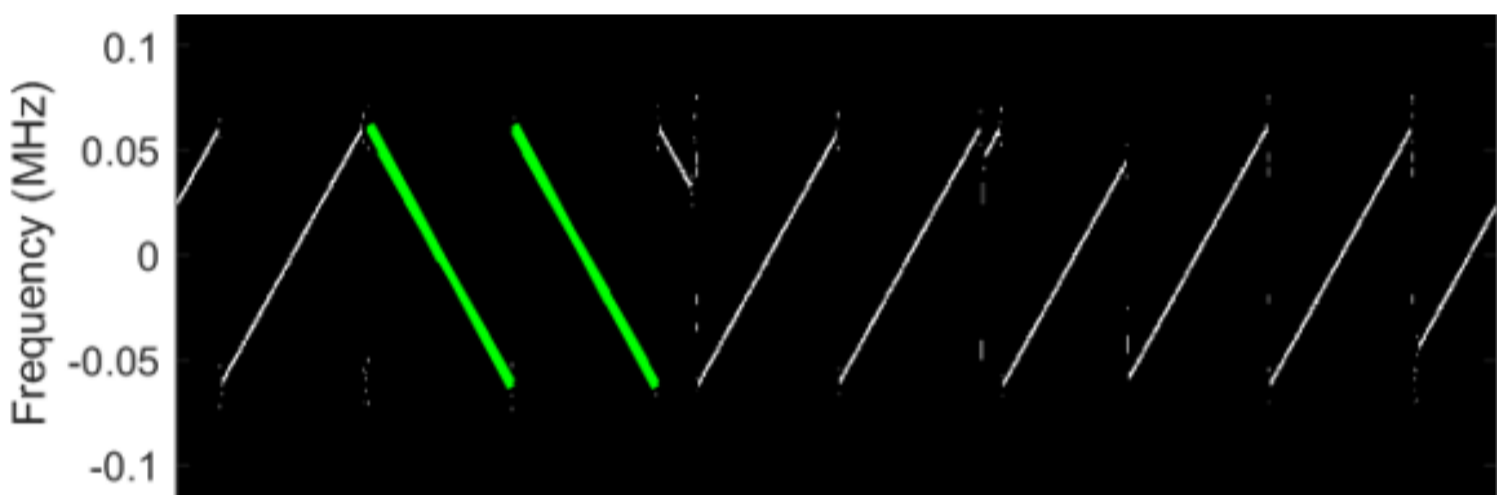


Fig 4: Detected Downchirps Overlaid on Thinned Image

HARDWARE SPECS

This new FPGA system has very impressive specifications. With 8 channels on both transmit and receive it has the potential to be a modular digital backend for a wide range of RF sensing solutions.

Zynq Ultra Scale +RFSoc Specs	
No of DAC / ADC Bits	14 / 12-bit
No of channels	8
ADC Sample Rate	4.096 GSPS
DAC Sample Rate	6.554 GSPS
System Logic Cells (K)	930
Memory (Mb)	60.5
DSP Slices	4272
Processors	Arm Cortex-A53 & Arm Cortex-R5

Table 1: Hardware Specs

The ARESTOR platform is based around the RFSoc hardware, combined with an in-house infrastructure and various IP blocks to create an RF sensing tool which can be configured for different sensing applications such as active radar, passive radar and electronic surveillance.

FUTURE WORK

This project will now look to expand situational awareness beyond LoRa transmissions to other IoT protocols of interest.

Alternative processing techniques, in particular processing based on machine learning (see Alan Turing Institute partnership below) could also be implemented within the real-time ML framework.

PROJECT TIMELINE

Start date: Jan 2022
End date: July 2022

USER PARTNERS

Dstl are a key partner within this project. They have provided context of the RF situational awareness. In addition, the Alan Turing Institute has partnered on Machine Learning (ML) processing techniques for application with RF signals.

ACKNOWLEDGEMENTS

This work has been supported by the PETRAS National Centre of Excellence for IoT Systems Cybersecurity, which has been funded by the UK EPSRC under grant number EP/S035362/1

